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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,111	INDO, SEIYA	
	Examiner	Art Unit	
	Emerson C Puente	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-9, and 13-15* is/are rejected.

7)☒ Claim(s) *4-6,10-12 and 16-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/5/03,6/27/03,5/7/03, 2/28/02*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-18 have been examined.

Information Disclosure Statement

The information disclosure statements filed 6/27/03 and 2/28/02 fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because they lack an English translation. It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-3,7-9, and 13-15 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 5,864,663 of Stolan in further view of US Patent No. 4,866,713 of Worger et al. referred hereinafter "Worger".

In regards to claim 1, Stolan discloses:

a controller which executes a reset process, in response to a reset signal (see column 2 lines 46-51);

an oscillator oscillates a clock (see column 2 lines 46-51 and column 5 lines 5-10); and

a timer which counts pulses of the clock, and outputs the reset signal to said controller, in a case where a counted value obtained by counting the pulses of the clock exceeds a predetermined limit value (see column 2 lines 49-55); and

wherein said controller controls said timer, and clears the counted value before the counted value exceeds the limit value (see column 3 lines 35-45), and

However, Stolan fails to disclose:

said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process.

Worger discloses

said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process (see column 4 lines 55-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made wherein said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process (see column 4 lines 55-60). A person of ordinary skill in the art would have been motivated because Stolan discloses a watchdog for detecting

failure to the microprocessor (see column 2 lines 50-53) and enabling a timer to start at the same time a reset process is initiated, as per teaching of Stolan, enables one to detect problems of the microprocessor during the reset process (see column 4 lines 65-67).

In regards to claim 2, Stolan discloses:

wherein said timer has a plurality of operational modes (see column 3 lines 62-67).

In regards to claim 3, Stolan discloses:

said controller outputs a mode specification signal for specifying an operational mode of said timer, to said timer; and said timer sets an operational mode thereof, in accordance with the mode specification signal (see column 3 lines 62-67).

In regards to claim 7, Stolan discloses:

a counter which counts pulses of a clock generated by an oscillator, and clears a counted value of the pulses, in response to a clear signal for designation to clear the counted value and being supplied from an external circuit (see column 3 lines 35-45 and column 5 lines 5-10); and

an output circuit which outputs a reset signal for designating to execute a reset process to said external circuit, in a case where the counted value exceeds a predetermined limit value (see column 2 lines 46-55), and

However, Stolan fails to disclose:

wherein said counter clears the counted value and begins counting the pulses of the clock in response to the reset signal output from said output circuit, thereby detecting an abnormal operation occurring in said external circuit during execution of the reset process.

Worger discloses

wherein said counter clears the counted value and begins counting the pulses of the clock in response to the reset signal output from said output circuit, thereby detecting an abnormal operation occurring in said external circuit during execution of the reset process (see column 4 lines 55-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made wherein said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process (see column 4 lines 55-60). A person of ordinary skill in the art would have been motivated because Stolan discloses a watchdog for detecting failure to the microprocessor (see column 2 lines 50-53) and enabling a timer to start at the same time a reset process is initiated, as per teaching of Stolan, enables one to detect problems of the microprocessor during the reset process (see column 4 lines 65-67).

In regards to claim 8, Stolan discloses:

wherein said watchdog timer has a plurality of operational modes (see column 3 lines 62-67).

In regards to claim 9, Stolan discloses:

further including a mode setting circuit which sets an operational mode of said watchdog timer, in accordance with a mode specification signal which specifies the operational mode and is provided from said external circuit (see column 3 lines 62-67).

In regards to claim 13, Stolan discloses:

counting pulses of a clock generated by an oscillator (see column 2 lines 46-48);

clearing a counted value of the pulses, in response to a clear signal which is provided from an external circuit and designates to clear the counted value (see column 3 lines 35-45); and

controlling said external circuit to execute a reset process, in a case where the counted value exceeds a predetermined limit value (see column 2 lines 49-55), and

Stolan fails to disclose:

wherein said counting includes detecting an abnormal operation occurring is said external circuit during execution of the reset process, by counting the pulses of the clock in synchronization with that said external circuit begins the reset process.

Worger discloses wherein said counting includes detecting an abnormal operation occurring is said external circuit during execution of the reset process, by counting the pulses of the clock in synchronization with that said external circuit begins the reset process (see column 4 lines 55-60).

It would have been obvious to one of ordinary skill in the art at the time the invention was made wherein said timer begins counting the pulses of the clock in synchronization with that said controller begins the reset process, thereby detecting an abnormal operation occurring in the computer during execution of the reset process (see column 4 lines 55-60). A person of ordinary skill in the art would have been motivated because Stolan discloses a watchdog for detecting failure to the microprocessor (see column 2 lines 50-53) and enabling a timer to start at the same time a reset process is initiated, as per teaching of Stolan, enables one to detect problems of the microprocessor during the reset process (see column 4 lines 65-67).

In regards to claim 14, Stolan discloses:

wherein said detection methods includes a plurality of modes (see column 3 lines 62-67).

In regards to claim 15, Stolan discloses:

setting a mode of the detection method, in accordance with a mode specification signal which is provided from said external circuit and species the mode (see column 3 lines 62-67).

Allowable Subject Matter

Claim 4-6,10-12, and 16-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

See PTO 892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (571) 272-3652. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5631.

Emerson Puente
11/8/04

ERT BEAUSOLIEL
PATENT EXAMINER
CENTER 2100